REMARKS

Claims 1-7, 10 and 12-17 remain pending in the Application. Claims 8-9 and 11 are cancelled. Applicant respectfully requests reconsideration in light of the remarks presented herein.

The present invention is directed to a cache controller for a microprocessor that executes multiple tasks concurrently. The cache controller manages the cache memory. The cache memory has multiple regions that store data blocks for each of the multiple tasks. During task execution, the cache controller receives from the microprocessor, addresses for data blocks stored in main memory. For each address, the cache controller searches all of the cache memory regions to determine if the cache memory also contains the data block. If the data block is not in the cache memory, the cache controller acquires the data block from the main memory and stores it in the cache memory region for that particular task.

Applicant's cache controller features a judgment unit that is not present in conventional cache controllers. The judgment unit searches all of the cache memory regions to determine if the cache memory has a data block needed by the microprocessor. The judgment unit has a cache "hit" when the needed data block is in any of the cache regions and the judgment unit has a cache "miss" when the needed data block is not in any of the cache regions. This feature contrasts with a conventional cache controller that searches for data blocks only in the cache memory region where data blocks for that particular task are stored and only has a cache "hit" when the data block is in that region. The conventional cache controller, unlike Applicant's cache controller, will have a cache "miss" when a needed data block is in a cache memory region other than the cache memory region used for that particular task.

Claims 1-3 and 10-17 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Handy* ("The Cache Memory Book") in view of *Suh et al.* ("Dynamic Cache Partitioning for Simultaneous Multithreading Systems") further in view of *Chiou et al.* (U.S. Pat. No. 6,370,622).

Handy discloses a cache controller that receives an address from a microprocessor (*Handy*, Figure 1.6). The cache controller manages a cache directory and a cache memory (*Handy*, Page 12, Line 15 – Page 13, Line 1). The cache directory and memory store data and addresses based on the cache strategy or policy (*Handy*, Page 13, Lines 5-13). The cache controller receives addresses from the microprocessor and determines whether the data is in the cache memory. If the data is not available in the cache memory, the cache controller may acquire the data from the main memory and store it in the cache memory. *Handy*, as the Office Action acknowledges, does not disclose a region management unit to manage regions in the cache (Office Action, Page 3, Lines 2-4). Applicant also notes that *Handy* is also silent as to searching and caching data in more than one region making Applicant's judging unit and caching unit undisclosed by *Handy* as well (*Handy*, Page 12, 51 and 52).

Suh discloses a method for dynamic partitioning of cache memory for multithreading systems (*Suh*, Abstract). *Suh's* method compares the miss statistics of each thread and computes a marginal gain of allocating another data block of memory for each of the threads (*Suh*, Section 3.1, Paragraph 1, Section 3.2 Paragraphs 1-2). The marginal gain statistics are used to partition the cache memory (*Suh* Section 3.3 and 3.4). However, as acknowledged by the Office Action, *Suh* as well as *Handy* fail to teach, Applicant's judging unit (Office Action, Page 3, Lines 11-12).

Chiou discloses a device that allows software, firmware or hardware to dynamically restrict data to some subset of the cache and to dynamically specify a replacement algorithm for use with that subset (*Chou*, Figure 8, Column 17, Lines 57-61). *Chiou* refers to this feature as

cache mapping (*Chiou*, Column 17, Lines 60-61). The cache map may be implemented as a column cache with "each way" of the map represented as a set associative column (*Chiou*, Column 18, Lines 4-5). *Chiou's* cache is checked for a hit in the standard fashion (*Chiou*, Column 18, Lines 5-7). In the case of a miss, the retrieved data block may be placed into a specific column based on the mapping information (*Chiou,* Column 18, Lines 7-13). The two way map columns of *Chiou,* map regions of the cache memory to regions of main memory and map regions of main memory to regions of the cache memory. Thus it is possible that a region of memory may score a hit for more than one process.

Claims 1, 14 and 15 recite "a judging unit (step) operable to judge whether the data stored at the received address is stored in the cache memory, by searching all of the plurality of regions in the cache memory." The Office Action correctly asserts that this limitation is not disclosed by *Handy* or *Suh* (Office Action, Page 3, Lines 11-12). The Office Action, however, asserts this limitation is taught by *Chiou* (Office Action, Page 3, Lines 11-21). Applicant traverses.

The Office Action asserts that *Chiou* teaches "searching all the column caches when the miss occurs," (Office Action, Page 3, Lines 14-15). Applicant submits this is a misstatement of *Chiou's* teaching. *Chiou's* teaching more precisely states "in the case of a miss, the replacement cache line is determined using the standard replacement strategy but also taking into account cache mapping information," (*Chiou*, Column 18, Lines 7-10). There is nothing in this teaching that suggests searching all column caches when a miss occurs. Quite the contrary, the teaching suggests that the missing cache line is to be replaced using a standard strategy that takes into account the cache map.

Even if *Chiou* taught "searching all the column caches when the miss occurs" it would not disclose the recited limitation. "Searching all the column caches when the miss occurs" is a far cry from "judging whether the data stored at the received address is stored in the cache memory, by searching all of the plurality of regions in the cache memory."

Moreover, the asserted teaching would not be possible in the context of Applicant's claimed invention. Applicant's judging unit searches all of the plurality of regions in the cache memory. Thus a miss would not occur unless the entire cache memory was void of the data. This would make it unnecessary to employ the asserted teaching and "search all of the cache columns when a miss occurs."

The differences between the recited judgment unit and *Chiou* are important. Applicant's judgment unit provides for a cache controller that searches the entire cache memory. A cache hit will occur regardless of what region of the cache memory the desired data is stored in. In this way the cache controller is able to quickly retrieve any data that is stored in the cache memory.

In contrast, *Chiou's* cache controller will score a miss on data in cache memory that is not in the "retrieve" cache column. The cache data then must be retrieved from the main memory wasting precious processor time. Only after the time is wasted may *Chiou's* cache controller place the retrieved data in the cache memory taking in consideration the "store" cache column.

As explained above, *Handy, Su* and *Chiou* fail to disclose Applicant's recited judgment unit, making claims 1, 14 and 15 patentable over any combination of *Handy Su* and *Chiou.*

The Office Action relies on *Chiou* as the linchpin for the obviousness rejection. Yet the Office Action fails to show the motivation to combine the prior art teachings in the manner

claimed. The Office Action merely extols one of the virtues of Applicant's combination (i.e. increased performance) (Office Action, Page 3, Lines 19-20).

The Federal Circuit has held that a person of ordinary skill in the art must not only have had some motivation to combine the prior art teachings, but some motivation to combine the prior art teachings in the particular manner claimed. *See, e.g., In re Kotzab*, 217 F.3d 1365, 1371 (Fed. Cir. 2000) ("Particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination *in the manner claimed.*" (emphasis added)); *In re Rouffet*, 149 F.3d 1350, 1357 (Fed. Cir. 1998) ("In other words, the examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination *in the manner claimed.*" (emphasis added)).

The lack of a prior art teaching, suggestion or motivation to combine *Chiou*, with *Handy* and *Su* renders claims 1, 14 and 15 even more patentable over *Handy* in view of *Suh* further inv view of *Chiou*.

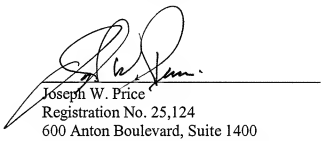
Claims 2-7, 10, 12-13 and 16-17 depend from claims 1, 14, and 15 and are patentable for the same reasons as claims 1, 14, and 15. Accordingly, Applicant respectfully requests that this rejection be withdrawn.

In light of the comments presented above, Applicant believes the Application is in condition for allowance.

If the Examiner believes that a telephone interview will help further the prosecution of the case, the undersigned attorney can be contacted at the listed telephone number.

Very truly yours,

SNELL & WILMER L.L.P.



Joseph W. Price
Registration No. 25,124
600 Anton Boulevard, Suite 1400
Costa Mesa, California 92626-7689
Telephone: (714) 427-7420
Facsimile: (714) 427-7799